Theoretical and Experimental Results of Substrate Effects on Microstrip Power Divider Designs

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ABSTRACT

The effects of substrate materials on the design of microstrip power divider are investigated theoretically and experimentally. Three different dielectric substrate materials are chosen ; Duriod 3003, G10/FR4 epoxy Glass and Duriod 3010 to be studied. A three-way double-stage power divider is designed at S-band frequency of 2.25 GHz and etched on each studied substrate separately. The substrate effects of large difference in dielectric constant and the dissipation factor ; on the characteristics and performance of the microsrip circuits are taken into consideration in the present study. The circuit designs presented here, are analyzed using the Genesys CAD program and implemented and tested experimentally. The simulated and measured results are compared , discussed and indicate that significant changes in the characteristics of the microstrip power divider are observed.

KEYWORD: Power divider, microstrip line, VSWR, isolation loss.

النتائج النظرية والعملية لتأثيرات طبقة الأساس في تصاميم موزعات القدرة ذات الاشرطة الدقيقة

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الملخص

تم بحث تأثيرات طبقة الأساس على تصاميم موزعات القدرة ذات الاشرطة الدقيقة نظريا وتجريبيا. تم اختيار ثلاث قواعد وهي: ديوروید 3003 , الزجاج الأبوكسي نوع G10/FR4 وديوروید 3010. وقد صممت ثلاثة موزعات قدرة مختلفة تختلف بأختلاف القاعدة حيث يتكون الواحد منها من مرحلتين وبثلاثة مخارج . وقد تم تصميم هذه الموزعات لتعمل عند التردد 2.25 GHz من الحزمة الترددية S . لقد تم تحليل الدوائر المصممة الثلاث بأستخدام برنامج Genesys CAD وبعدها تم تصنيعها وفحصها عمليا. تم مقارنة النتائج المستحصلة ومناقشتها وقد لوحظ بأن هناك تغييرات واضحة بخواص هذه الموزعات.

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1. Introduction

The power divider technology has undergone a substantial change over the past decade, due to smaller size, lighter weight, potentially lower cost, high reliability, broad bandwidth capability and function reproducibility [1,2]. When selecting a suitable substrate material, factors to be considered in the designs of the microstrip power dividers, are; cost, availability, ease of machining and etching. There are a whole range of mechanical, electrical, thermal and chemical criteria to be taken into account [3,4]. Most of these criteria are: mechanical stability with high and low storage temperature, thermal expansion similar to that of metals, good electrical properties (homogeneity of ε_r and high electric insulation strength), chemical resistance and easily workable with low cost [3]. There is no substrate material that simultaneously fulfils all the above requirements. The best compromise must be found for all applications [5]. The materials commonly used for microwave substrate have dielectric constants typically range from 2.0 to 10.0. Microstrip circuits designed to be fabricated on such dielectric materials will be most compact or pressed because of the wave-slowing action of the electric signal. Usually, this is an advantage, but such small size makes it difficult to fit any conventional discrete parts into microstrip layout. There are Teflon / ceramic mixture with lower dielectric constants, such as 6.0, which produce physical layer microstrip layout; this helps to alleviate the components mounting problem [6].

The present study investigates the effects of the dielectric substrate materials on the design of microstrip power dividers on which they are etched. Duriod 3003, G10/FR4 epoxy glass and Duriod 3010 substrates are chosen to be studied. The effects of the differences in the dielectric constants and the dissipation factors on circuit design are included.

2. Microstrip Power Divider Designs

A schematic diagram of the two-stage Wilkinson N-way divider is shown in figure 1.

The common port is designated the number 0, and is assumed to be terminated in Z_c. The divider ports are designated the number 1 through N, and each is terminated in Z_d. The characteristic impedance of each quarter-wave line is $Z_{0,1}$ and $Z_{0,2}$ while the isolation resistors are designated R_1 and R_2. The justification for the coupling among all transmission lines beyond the first stage of the divider, is that such lines would be reasonably separated from one another [7]. Also the junction effects will be neglected. It will be assumed that port 0 (input port) is perfectly matched at the center frequency. Thus, for two-stage hybrid:

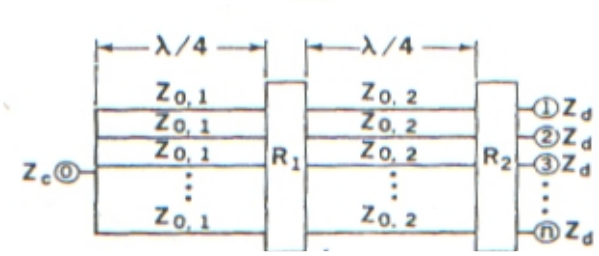


Figure 1: Schematic representation of two-stage power divider

$$Z_{0,1} = Z_{0,2}(NZ_c/Z_d)^{1/2} \quad (1)$$

Where Z_c and Z_d are the input and output impedances of the power divider respectively. For a maximally flat input-output frequency response, the following impedances are:

$$Z_{0,1} = (NZ_c)^{3/4}\,(Z_d)^{1/4} \quad (2)$$

$$Z_{0,2} = (NZ_c)^{1/4}\,(Z_d)^{3/4} \quad (3)$$

The addition of input and output transformers to improve the frequency response is allowed provided that Eq.(1) is satisfied with Z_c and Z_d referred to terminals of the dividers[7]. Table.1 represents the optimum resister of two-stage N-way power divider [7].

Table 1: Optimum resistors of two-stage N-way power divider[7].

N	$\left[\frac{R_1 Z_d}{Z_{0,2}}\right]_{opt}$	$(\frac{Z_d}{R_2})_{opt}$
2	1.28719	0.17828
3	0.75000	0.25000
4	0.50000	0.25000
5	0.39991	0.33609
6	0.36676	0.36285
7	0.39652	0.35000
8	0.52493	0.30118
10	0.52482	0.30121
12	0.52483	0.30120

The characteristic impedance of the microstrip line Z_{0L} may be expressed in terms of line width w and substrate thickness h, and effective dielectric constant ε_e as [4]:

$$Z_{0L} = \begin{cases} \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) & for\ \frac{w}{h} \leq 1 \\ [120\pi]\ [\sqrt{\varepsilon_e}\ (\frac{w}{h} + 1.393 + 0.677 \ln\ (\frac{w}{h} + 1.44))]^{-1} & for\ \frac{w}{h} > 1 \end{cases} \quad (4)$$

Where $$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} (1 + \frac{12h}{w})^{-1/2} \quad (5)$$

and ε_r represents relative dielectric constant of the substrate. The dielectric loss α_d is given by[4]:

$$\alpha_d = \frac{\pi}{\lambda_0} q\ tan\delta \qquad N_p/m \quad (6)$$

Where $q = \frac{\varepsilon_r(\varepsilon_e - 1)}{\varepsilon_e(\varepsilon_r - 1)}$ and $tan\delta$ represents dissipation factor.

Table 2 illustrates the specifications of the studied substrate materials with the dimensions of 50 ohms line for each one.

Table 2: Specifications of the studied substrates with the dimensions of 50 ohms line for each.

	Duriode 3003	**glass**	**Duriode 3010**
Dielectric constant ε_r	3	4.4	10.2
Dielectric thickness *h*	1.52 mm	1.6 mm	1.25 mm
Dissipation factor	0.0013	0.013	0.0035
Width of 50 ohms line	3.84 mm	2.47 mm	1.10 mm
Length of 50 ohms line	21.91 mm	18.42 mm	12.71 mm

(a) Power divider with Duriod 3003 and epoxy glass substrates

A 50 ohms , $\lambda_g/4$ line at mid band frequency of 2.25 GHz is 3.84 mm wide, 21,91 mm long for the Duriod 3003 substrate and 2.47 mm wide, 18.42 mm long for epoxy glass substrate. The main difference between these two substrates is the dissipation factor $(tan\delta)$. They are near in the dielectric constants and the thickness of the substrate, therefore the layout design is changed in the range of a few millimeters. The dissipation factor does not

affect the dimensions of the power divider design, its effect will be clear in the simulated and practical response curves.

Using equations (2) and (3), the impedance design values are: $Z_{0,1} = 113.975\ \Omega$, $Z_{0,2} = 65.803\ \Omega$, $R_1 = 64.954\ \Omega$ and $R_2 = 200\ \Omega$, with the input and the output impedances set at: $Z_{in} = Z_{out} = Z_d = Z_c = 50\ \Omega$.

Figure 2 shows the schematic diagram of power divider designed on Duriode 3003 or Epoxy glass substrate noticing that only the slight differences in the dimensions of the microstrip lines related to the change in dielectric constant and thickness of the used board.

Figure 3 and figure 4 illustrate the photograph of the designed power dividers etched on Duriode 3003 and epoxy glass substrates respectively.

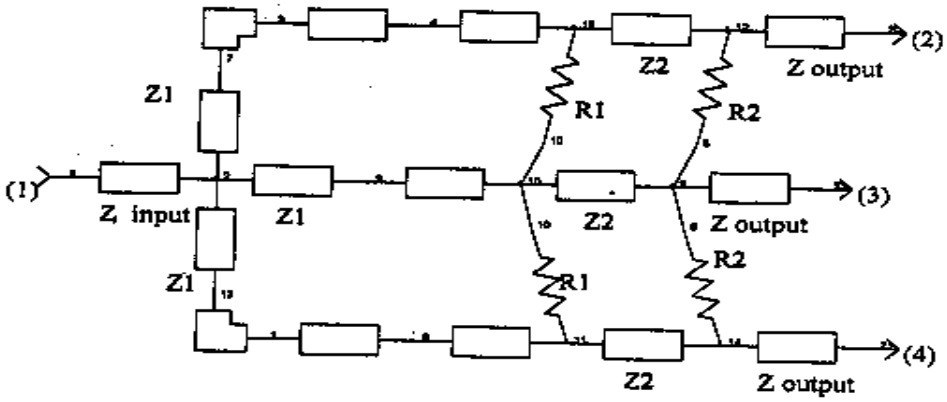


Figure 2: Schematic diagram of 3-way 2-stage power divider designed on Duriode 3003

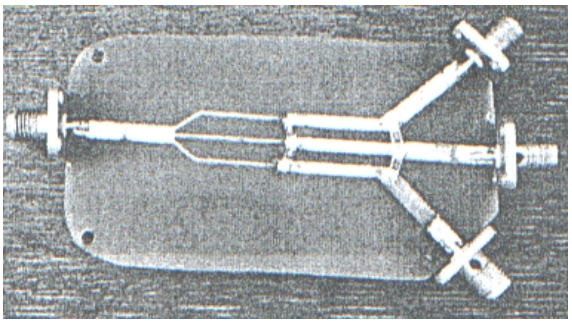


Figure 3: Picture of 3-way 2-stage power divider etched on Duriode 3003 board (Dim. 100 mm x 55 mm)

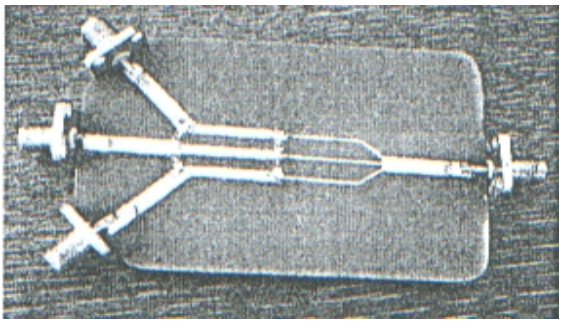


Figure 4: Picture of 3-way 2-stage power divider etched on epoxy glass board (Dim. 93 mm x 49 mm)

(b) Power divider with Duriod 3010

The main difference between this substrate and the other is the high dielectric constant. The comparison is with the Duriod 3003 because it has approximately the same dissipation factor. A 50 ohms, $\lambda_g/4$ line at mid band frequency of 2.25 GHz is 1.10 mm wide and 12.71 mm long. Following the same design procedure of power divider , the microstrip lines needed in the design are such thin that it is difficult to be fabricated; therefore the values of $Z_{0,1}$ and $Z_{0,2}$ are selected to give large dimensions

$Z_{in} = 25\ \Omega$, $Z_{out} = 19\ \Omega$, $Z_{0,1} = 53\ \Omega$, $Z_{0,2} = 26\ \Omega$, $R_1 = 22\ \Omega$, $R_2 = 76\ \Omega$.

An additional transformation matching line $\{B\}$ is inserted in the design to transform the impedance $\{A\}$= 25 Ω to 50 Ω line $\{C\}$ for matching purposes . Also an additional 30 Ω stub is inserted to transform 19 Ω output to the 50 Ω line as shown in figure 5. Figure 6 illustrates the photograph of the power divider etched on Duriode 3010 substrate.

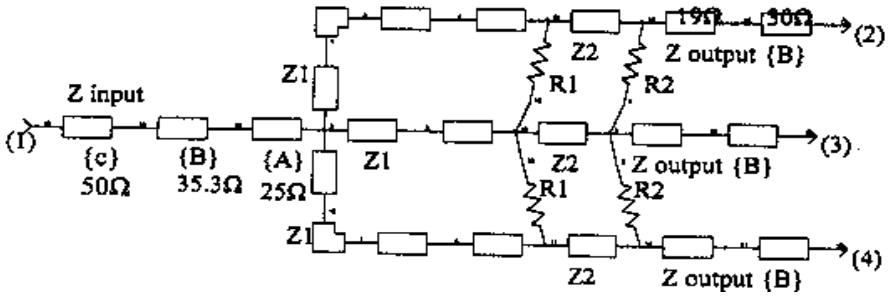


Figure 5: Schematic diagram of 3-way 2-stage power divider designed on Duriode 3010

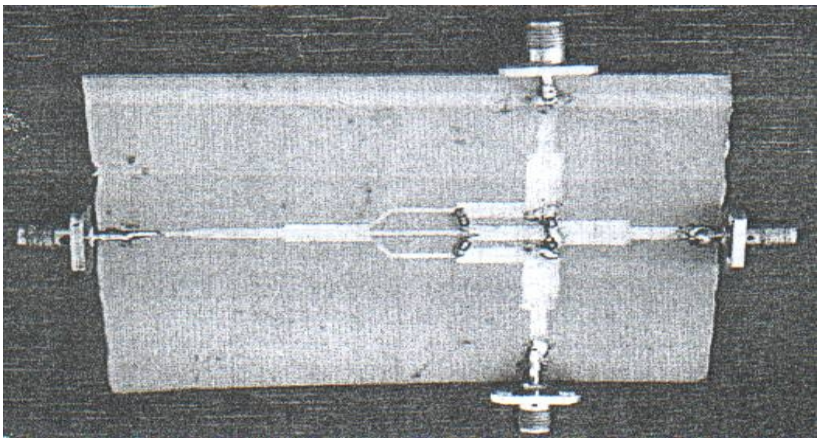


Figure 6: Picture of 3-way 2-stage power divider etched on Duriod 3010 board (Dim. 110 mm x 90 mm)

3. EXPERIMENTAL SUT-UP

The implemented designs of the studied microstrip power dividers are tested and their characteristics are found by using the network analyzer 8510 HP as pictured in figure 7. The network analyzer has two ports (1 and 2) that are connected respectively to the input and one of the outputs of the tested power divider, while the remaining outputs of the power divider are connected to 50 Ω load for each. Voltage standing ratio VSWR, the coupling and the isolation between the power divider input and each output are measured by connecting the power divider input (representing port 1 of a device under test DUT as shown in figure 8) to port 1 of the network analyzer (a_1 and b_1) , while the each

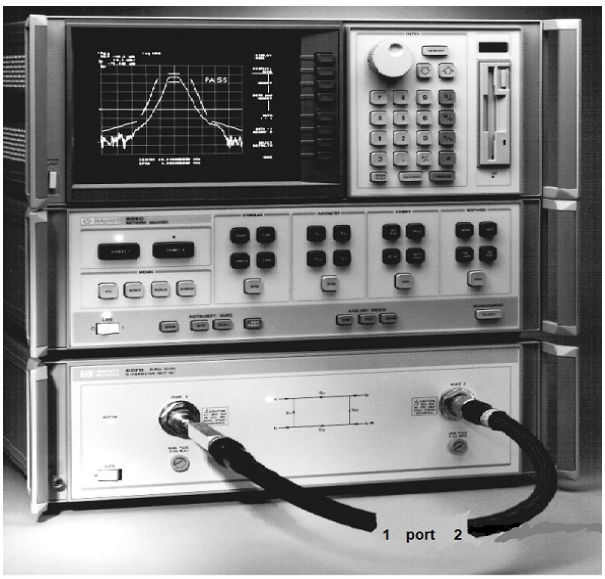


Figure 7: The used network analyzer 8510 HP

power divider output representing port 2 of DUT is connected to port 2 of the network analyzer (a_2 and b_2). a_1 and b_1 represent the incident and reflected or received voltage signals respectively at port 1 while a_2 and b_2 are the incident and reflected or received voltage signals respectively at port 2 of the network analyzer. Based on this set-up, the following parameters are measured and the results are displayed directly on the analyzer [4]:

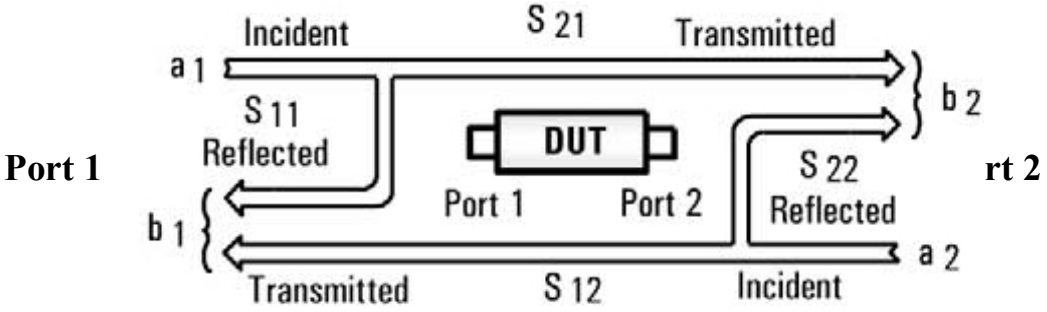


Figure 8: Block diagram of the experimental set-up

(a) S_{11} Represents the forward reflection coefficient and $S_{11} = b_1/a_1$, $a_2 = 0$.

(b) Input VSWR represents the input match and $VSWR = \frac{1+S_{11}}{1-S_{11}}$.

(c) S_{22} Represents the reverse reflection coefficient and $S_{22} = b_2/a_2$, $a_1 = 0$.

(d) Output VSWR represents the output match and $VSWR = \frac{1+S_{22}}{1-S_{22}}$.

(e) S_{21} Is the forward transmission coefficient that represents the coupling between the input and output ports and $S_{21} = b_2/a_1$ when $a_2 = 0$.

(f) S_{12} Is the reverse transmission coefficient that represents the coupling between the input and output ports and $S_{12} = b_1/a_2$ when $a_1 = 0$.

The above procedure is repeated for each tested output of the studied power divider taking into consideration that the calibration of the network analyzer ports should be made before the test beginning, regarding that the reference planes are taken at the power divider ports.

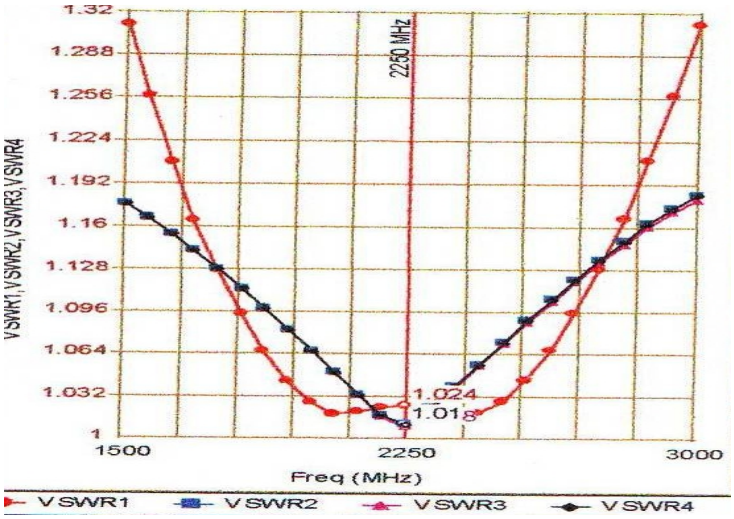
4. RESULTS AND DISCUSSION

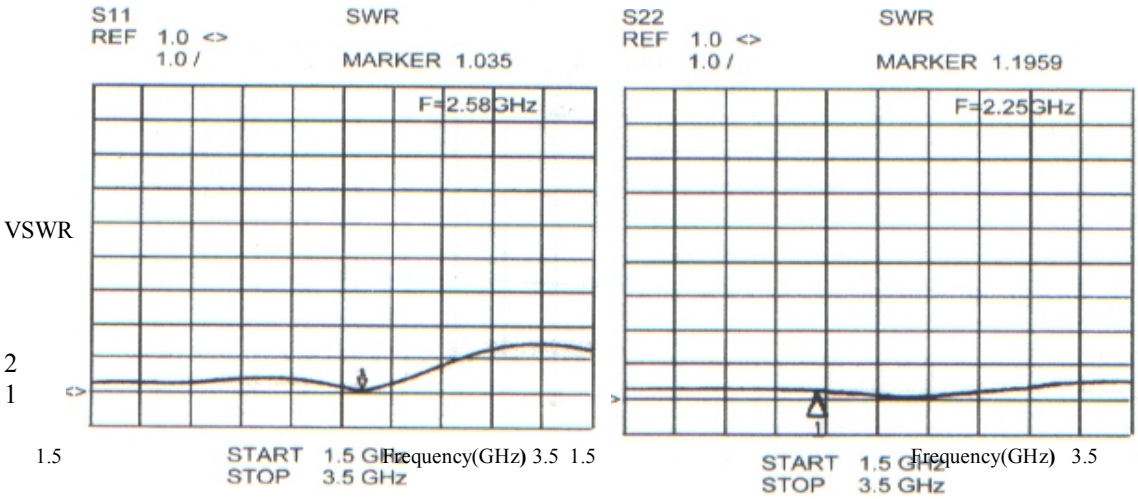
By the aid of Genesys software package, the previous three designs of microstrip power dividers etched on the studied substrates are simulated and implemented. The characteristics of the implemented designs are determined using the experimental set-up discussed in section 3. Figure 9 shows the simulated and the measured VSWR.

The input VSWR is varying and less than 2:1 for frequency range 1.3-2.95 GHz, while the output VSWR is between 1 and 1.5 for the studied frequency range 1.5-3.5 GHz.

Figure 10 illustrates the coupling of the power divider printed on Duriode 3003.

Figure 9 (a)





(b) (c)

Figure 9: Response curves of 3-way 2-stage power divider printed on Duriode 3003 substrate. (a) Simulated input and output VSWR,(b) and (c) measured input and output VSWR respectively

Figure 10(a)

Measured coupling (dB)

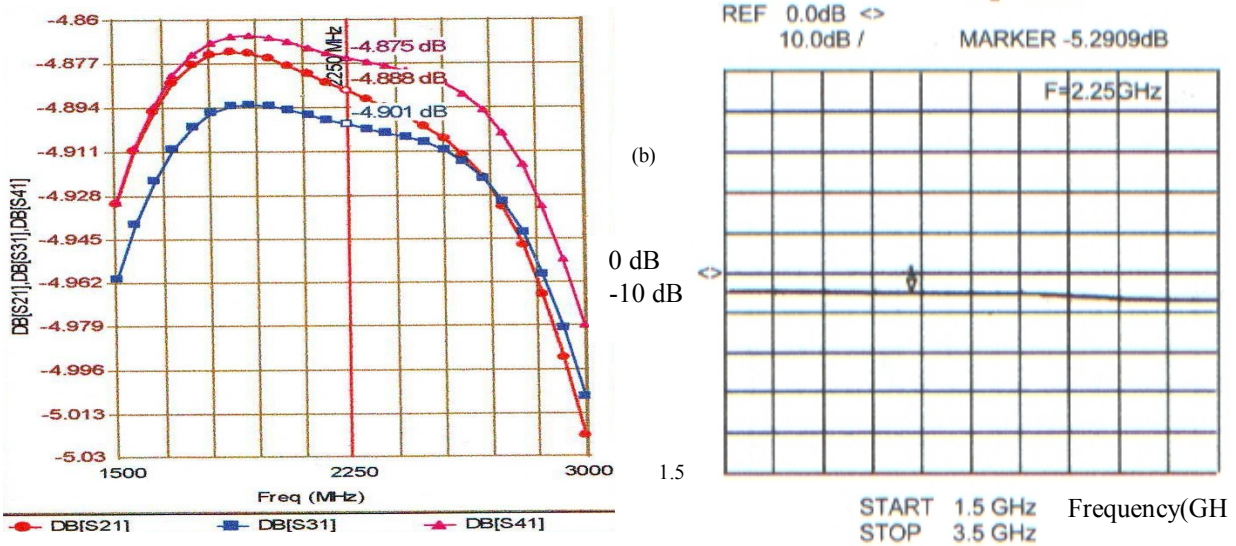


Figure 10: Response curves of 3-way 2-stage power divider printed on Duriode 3003 substrate.(a) simulated coupling,(b) measured coupling.

The isolation parameter of power divider is shown in figure 11. Agreement is found between the simulated and measured results, in term

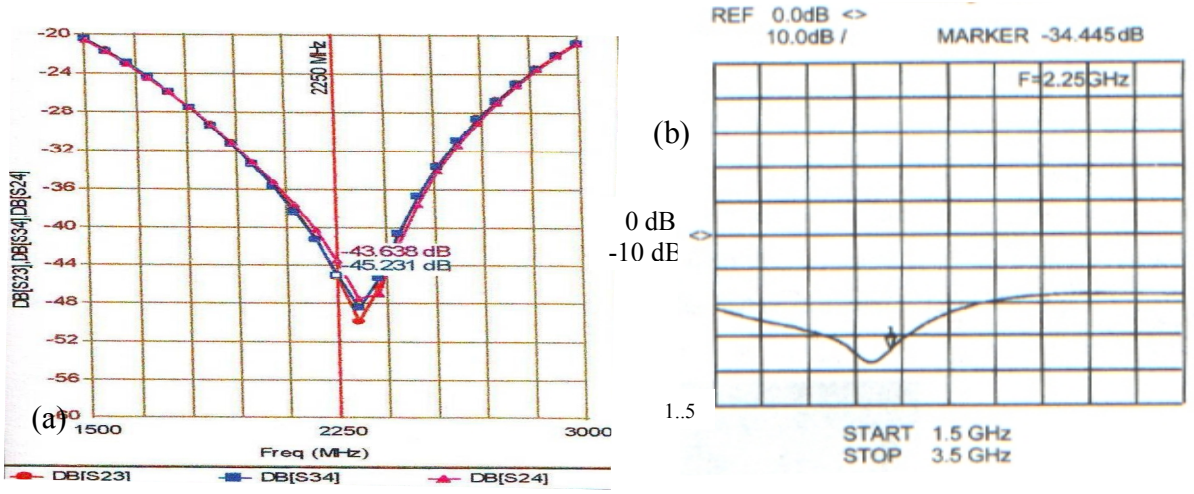
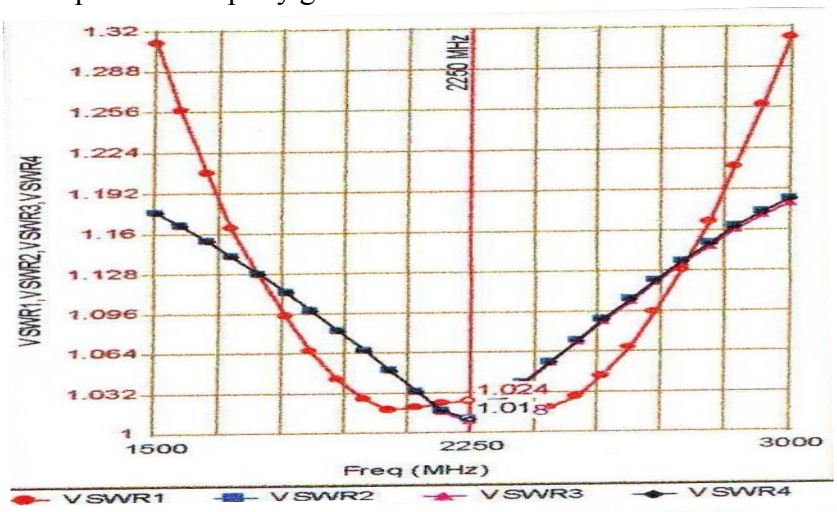


Figure 11: Response curves of 3-way 2-stage power divider printed on Duriode 3003 substrate.(a) simulated isolation, (b) measured isolation

The corresponding figures to those of the first prototype are shown in figures 12,13 and 14 for the power divider printed on epoxy glass substrate.

Figure 12(a)



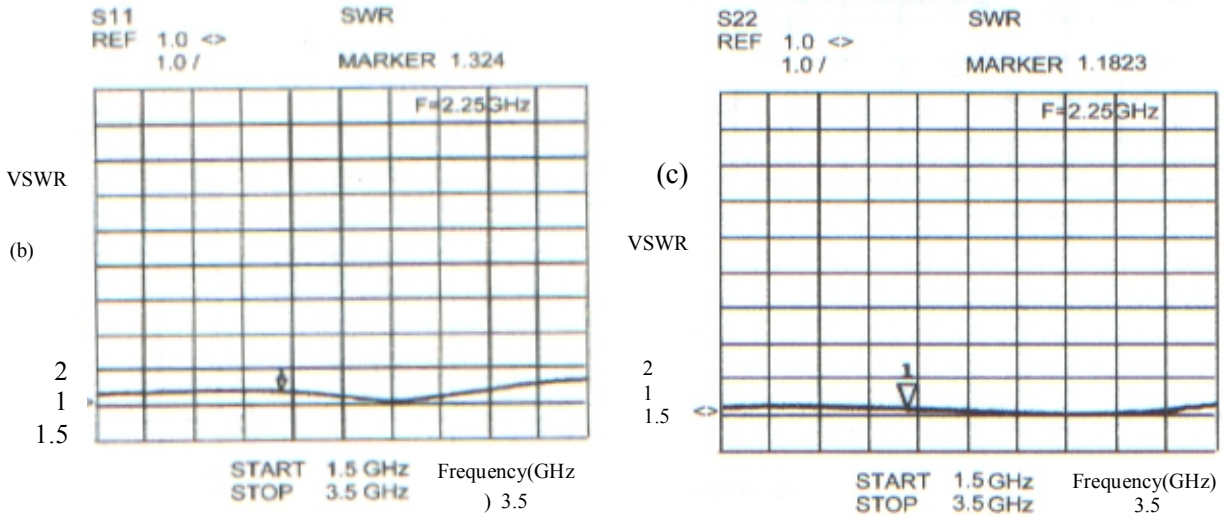


Figure 12: Response curves of 3-way 2-stage power divider printed on epoxy glass substrate

(a) simulated input and output VSWR,(b) and (c) measured input an Measured coupling (dB) ly

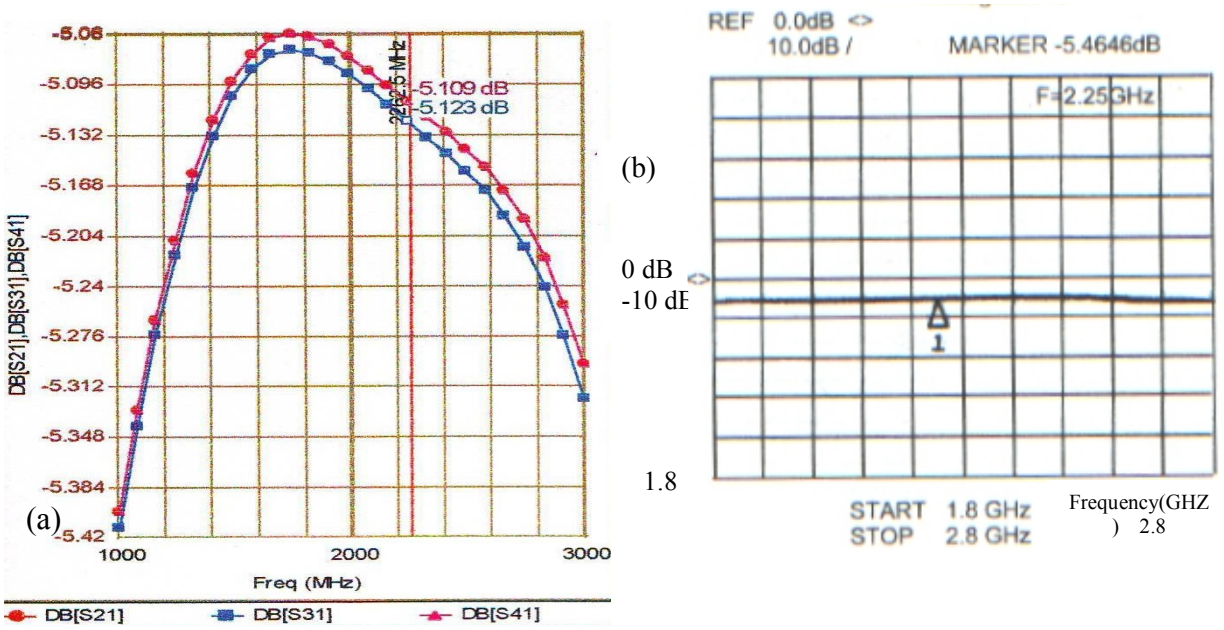
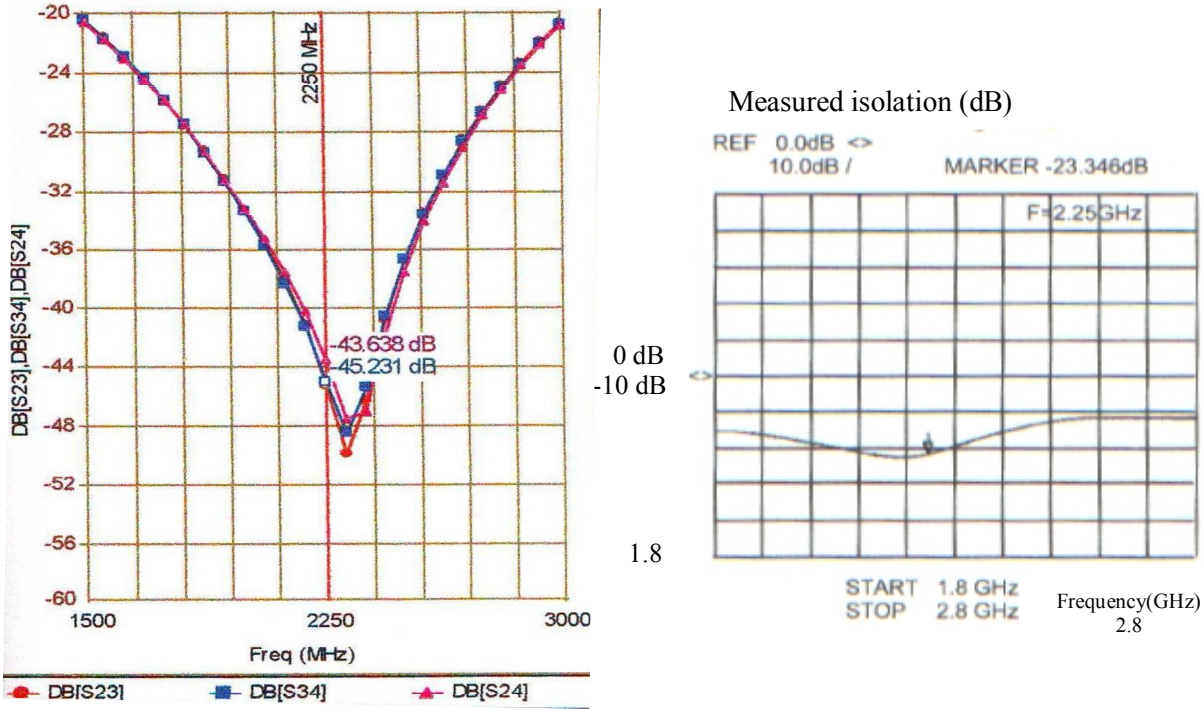


Figure 13: Response curves of 3-way 2-stage power divider printed on epoxy glass substrate.(a) simulated coupling,(b) measured coupling.

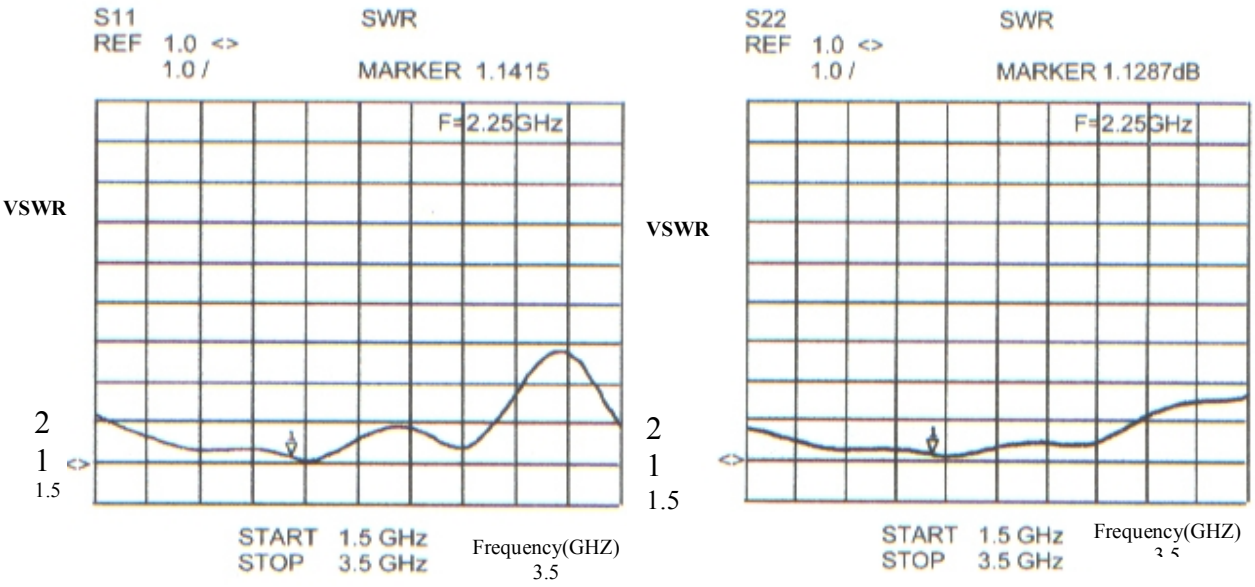


(a) (b)

Figure 14: Response curves of 3-way 2-stage power divider printed on epoxy glass substrate.(a) simulated isolation,(b) measured isolation.

It can be seen that the increasing in the split ratio indicates there is more power lost compared to the first one and is related to higher dissipation factor in the second substrate.

Figures 15, 16 and 17 represent the simulated and measured VSWR, coupling and isolation of the third prototype etched on Duriode 3003 respectively.



(a) (b)

Figure 15: Response curves of 3-way 2-stage power divider printed on Duroide 3010 substrate.(a) measured input VSWR and (b) measured output VSWR

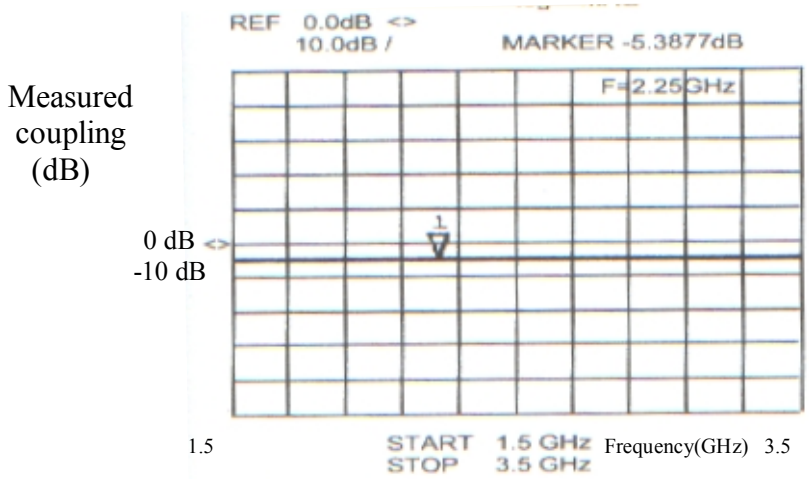


Figure 16: Measured coupling curve of 3-way 2-stage power divider printed on Duroide 3010 substrate

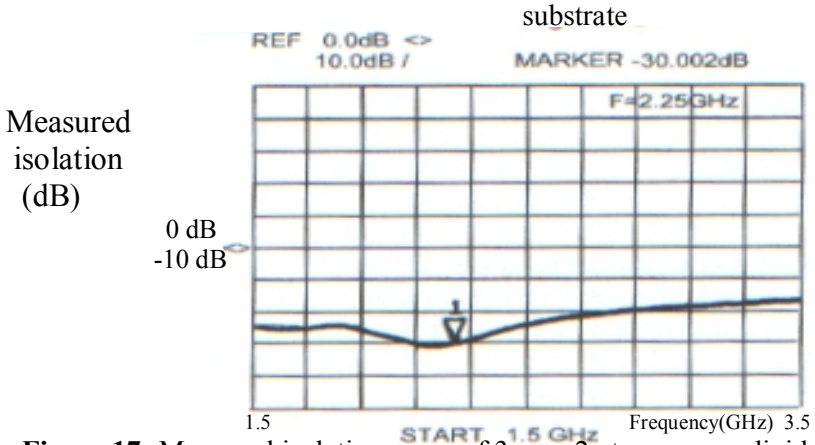


Figure 17: Measured isolation curve of 3-way 2-stage power divider printed on Duroide 3010 substrate.

It is clear that the measured coupling curves agree with the computed curve and the coupling remains less than -5.3 dB for different ports over the major part of the studied frequencies. The measured results are satisfactory.

It is seen that the most measured results presented in this study have a small shift in the center frequency , this is related to the etching that does not give the exact dimension of the lines. Table 3 compares the obtained results of the main parameters of the studied substrate materials.

Table 3: Comparison of the studied substrates at 2.25GHz

	Duriod 3003	**Epoxy glass**	**Duriod 3010**
Input VSWR	1.4	1.3	1.14
Output VSWR	1.19	1.18	1.12
Coupling (dB)	-5.3	-5.4	-5.38
Isolation (dB)	-34	-23.9	-30

5. Conclusion

The present study has introduced and discussed the effects of three different substrate materials: Duriode 3003, epoxy glass and Duriode 3010, on the characteristics of three-way double stage microstrip power dividers. The effects of large difference in dielectric constant and the dissipation factor on the circuit design properties have been observed as indicated in Table 3. The availability of the substrate material, its price, the size required, the number of divider needed, and generally the cost are the main parameters to fulfill the design requirements.

6. References

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The work was carried out at Sulaimani Technical College